

SYSTEM AND METHOD TO TEST INTEGRATED CIRCUITS ON A WAFER

Abstract

A system to test integrated circuits on a wafer may include a transceiver formed on the wafer. The system may also include an antenna system couplable to the transceiver. The transceiver may be formed in one of a scribe line on the wafer, a chip on the wafer or on an usable portion of the wafer. The antenna system may be formed in at least one of the same scribe line as the transceiver or in at least one other scribe line formed in the wafer. Alternatively, the antenna system may include an antenna external to the wafer.